PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte Furukawa

Appeal No. _____

Appellant:	Furukawa et al.	Confirmation No.:	5663
Serial No.:	10/767,065		
Filed:	January 29, 2004		
Art Unit:	2811		
Examiner:	Ori Nadav		
Title:	**VERTICAL NANOTUBE SEMICONDUCTOR DEVICE STRUCTURES AND METHODS OF FORMING THE SAME**		
Attorney Docket:	ROC920030268US1		

Cincinnati, OH 45202 February 2, 2011

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Sir:

REPLY BRIEF

I hereby certify that this correspondence for Application No. 10/767,065 is being electronically transmitted to Technology Center 2811, via EFS-WEB, on February 2, 2011.

/William R. Allen/
William R. Allen, Reg. No. 48,389

February 2, 2011
Date

I. Status of the Claims

Claims 1-6 and 8 are pending, stand rejected, and are now on appeal. Claims 7 and 9-34 have been cancelled.

II. Grounds of Rejection to be Reviewed on Appeal

1. Claims 1-6 and 8 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,566,704 to Choi.

III. Argument

The Appellant respectfully submits that the Examiner's rejection of claims 1-6 and 8 is not supported on the record, and that the Board should reverse the rejection.

On pages 7 and 8 of the Answer, the Examiner presents remarks regarding a comparison between "physical coupling" and "electrical coupling". Claim 1 recites that each of the semiconducting nanotubes includes "a first end electrically coupled with said source region" and "a second end electrically coupled with said drain region". As discussed on page 5 of the Appellant's Appeal Brief, "Figures 1-3 of Choi fail to show a second nanotube that is electrically coupled with the source region (40) and drain region (50) to which the depicted nanotube (100) is electrically coupled." In Figures 1-3, Choi fails to show a second nanotube that is either electrically or physically coupled with the source region (40) and the drain region (50) to which nanotube (100) is electrically coupled. Consequently, Figures 1-3 of Choi fail to disclose more than one nanotube (i.e., "a plurality of nanotubes") each having one end electrically coupled with the source region (40) and another end electrically coupled with the drain region (50).

Claim 1 also recites that each of the semiconducting nanotubes includes "a channel region extending vertically through said gate electrode between said source region and said drain region" and that the gate electrode is "configured to receive a control voltage effective to regulate current flow through said channel region between said source region and said drain region". Claim 1 clarifies that the electrical coupling of each semiconducting nanotube with the source and drain regions results in current flow through the channel region between the source and drain regions. The Examiner's construction of the claim term "electrically coupled" is unreasonable because the Examiner's construction divorces the term from the physical effect of the electrical coupling that is also recited in claim 1. The Examiner relies on this overly broad claim construction when interpreting Choi. In Choi, a pair of unit cells constructed as in figures 1-3 and electrically coupled to, for example, the same source region (40) will be electrically coupled to different drain regions (50) so that each of the two unit cells can be individually addressed. Carriers flowing from the source region (40) through the channel region of the nanotube (100) of one of the unit cells to its drain region (50) will not flow through the channel region of the nanotube (100) of the other unit cell in the pair.

The claim term "electrically coupled" is used in claim 1 in a manner that is consistent with the Appellant's specification. The Appellant's specification describes the result of the electrical coupling of each drain contact (40) with the nanotubes (14) and each source contact (38) with the same nanotubes (24) is that "[c]arriers flow selectively from the catalyst pad 10 through the carbon nanotubes 14 to the drain contact 40 when an electrical voltage is either *(sic)* applied via the corresponding gate contact 36 to one of the gate electrodes 30 to create a channel in the carbon nanotubes 14 extending therethrough".

Hence, the Examiner is interpreting the claim term "electrically coupled" in an overly broad manner that is unreasonable in view of the plain language of the claim and the Appellant's specification.

With regard to the Examiner's remarks on page 8 of the Answer, the Examiner initially comments that "claims 1-6 and 8 stand rejected over the embodiment of figures 1-3 of Choi et al., and not over the embodiment of Figure 4B". Because the Examiner admits in the Answer that claims 1-6 and 8 are not rejected over the embodiment of Figure 4B, then the Examiner did not use the embodiment of Figure 4B in his *Graham* analysis. Accordingly, the Board should disregard the disclosure contained in Figures 4A and 4B of Choi when assessing the Examiner's analysis of the ground of rejection.

In the event that the Board disagrees with the Appellant regarding the Examiner's admission and proceeds to consider the Examiner's comments in the Answer regarding his purported *Graham* analysis Figures 4A and 4B of Choi, the Examiner further states on page 8 of the Answer that "it is clear that figure 4A plurality of nanotubes are electrically coupled ... between one source region 40 and one drain region 50". The Appellant disagrees.

With regard to FIG. 4B, Choi discloses that "a source line and a drain line intersect at locations where the carbon nanotubes are grown to form unit cells". *See* col. 4, lines 55-58. Choi fails to provide any indication in Figure 4B signifying the location for the cross-sectional view of Figure 4A. The cross-section of Figure 4A in Choi fails to correspond to any cross-section that could be taken in Figure 4B of Choi as the number of nanotubes and the locations of the source region and drain region shown in Figure 4B are inconsistent with Figure 4A. However, Choi discloses that "FIGS. 4A and 4B illustrate a vertical cross-sectional view and a

perspective view of a vertical nano-sized transistor using carbon nanotubes according to a second embodiment of the present invention". *See* col. 3, lines 1-4. Because Choi discloses only a single embodiment is displayed in Figures 4A, 4B, the disclosure contained in Figure 4A of Choi is directly contradictory to the contained in Figure 4B of Choi and, even if the Board disregards the Examiner's admission of non-reliance on the embodiment of Figures 4A and 4B in the rejection, the disclosure associated with in Figures 4A, 4B of Choi is an unreasonable basis to reject claims 1-6 and 8.

With further regard to the Examiner's remarks on page 8 of the Answer, the Examiner considers Figure 4B in Choi (even if the Board disregards the Examiner's admission in the Answer of non-reliance on the embodiment of Figures 4A and 4B in his *Graham* analysis) to disclose "one device comprising a plurality of nanotubes 100, four source regions 40 and four drain regions 50". The Examiner continues that "[s]ince all the elements of the transistor are electrically coupled to each other, then the plurality of nanotubes 100 are electrically coupled between one source region and one drain region". None of the nanotubes (100) visible in Figure 4B is coupled with the same source region (40) and the same drain region (50) as any other of the nanotubes (100). The source and drain regions (40, 50) are laid out in grid so that each unit cell containing a single nanotube (100) can be individually addressed. Each nanotube (100) has its own source region (40) and its own drain region (50). When the a voltage is applied to the gate (20), carriers flowing as a current through any one of the nanotubes (100) visible in Figure 4B does not flow through any of the other nanotubes (100) visible in Figure 4B. The direction of current flow for the carriers in each of the nanotubes (100) is from its source region (40) to its drain region (50), or vice versa. Carriers flowing in this manner through any one of the nanotubes (100) do not flow through any of the other nanotubes (100).

Claim 1 also requires that the electrical coupling is configured such that control voltage on the gate electrode is "effective to regulate current flow through said channel region between said source region and said drain region". Because the gated current of carriers only flows in one direction through the nanotubes (100) in Figure 4B of Choi, no pair of nanotubes (100) visible in Figure 4B is "electrically coupled" with another of the nanotubes as claimed.

With regard to the Examiner's remarks on page 9-12 of the Answer, the unit cell shown in Figures 1-3 is a complete transistor containing a source region (40), a drain region (50), a gate (20), and a nanotube (100). No additional structure is needed to define a working transistor. The Examiner states that "practical devices do not comprise one unit cell but *(sic)* plurality of unit cells". A "practical device"[1] addresses the unit cells individually, not as a group. All of the unit cells in a "practical device" are not addressed using one source region and one drain region, as contended by the Examiner in the May 5, 2010 Office Action and in the Answer. In this scenario, the practical device would only have a single bit. Instead, each of the unit cells in Choi is addressed individually. This is how, quoting the Examiner, "a chip, which is practical device, comprising 'many thousands to millions of FETs" can contain thousands and millions of units cells as in Figures 1-3 of Choi that are individually addressed to provide the functionality of a device such as recited by Choi at "column 1, lines 29-38". The Appellant is not contending that Choi contains a single unit cell, but instead that Choi contains "many thousands to millions of FETs" each constructed like the unit cell described in connection with Figures 1-3 of Choi and that none of these unit cells has the same source region and the same drain region as another of the unit cells so that each of the unit cells in Choi can be individually addressed.

On Pages 10 and 11 of the Answer, the Examiner quotes passages from columns 1 and 2 of Choi. However, these passages are found in the Background and Summary sections of Choi and are inconsistent with the disclosure in Figures 1-3 of Choi that is used by the Examiner in his *Graham* analysis of claim 1. Any attempt to interpret the disclosure in Figures 1-3 of Choi based upon the passages from the Background and Summary sections of Choi leads to irreconcilable inconsistency with the actual disclosure in Figures 1-3. As Choi is construed by the Appellant, the disclosure in Figures 1-3 of Choi is of a unit cell that forms a complete functional transistor and that contains a single nanotube (100). The Appellant respectfully submits that the disclosure in Choi is more susceptible to the interpretation ascribed to the disclosure in Figures 1-3 of Choi, as explained herein and as explained in the Appellant's October 4, 2010 Appeal Brief, that the embodiment shown in Figures 1-3 of Choi should be interpreted as showing a functional transistor that includes only a single nanotube (100), and that the Examiner's construction that

[1] Quoting the Examiner from the Answer.

the embodiment shown in Figures 1-3 of Choi includes multiple nanotubes is objectively unreasonable.

On page 12 of the Anwer, the Examiner states that "[a]n artisan will not change the construction the unit cell depicted in figures 1-3". This emphasizes that the Examiner is not modifying the unit cell, but somehow attempting to justify grouping multiple unit cells into a transistor structure when Figure 4B of Choi is clear that no pair of nanotubes (100) shares the same source region (40) and the same drain region (50). In the event that the Board elected to consider the Examiner's comments in the Answer regarding his purported *Graham* analysis Figures 4A and 4B of Choi disclosure despite his admission in the Answer, the Examiner states on page 12 that "it is easier to operate the device when external connections are formed only to one drain region and to one source region, instead of connecting the external connections to plurality of drain regions and plurality of source regions". This statement disregards the addressing of individual unit cells that a person having ordinary skill in the art would understand is needed to form a "practical device". A person having ordinary skill in the art would appreciate that connecting all of the nanotubes (100) of the different unit cells to a single source region and to a single drain region would make a one-bit device, which is not in the Examiner's words "practical".

On Page 14 of the Answer, the Examiner again contends that Figures 1-3 of Choi can be interpreted in a manner with which the Appellant disagrees for reasons set forth in the Appeal Brief. As discussed above, these passages are found in the Background and Summary sections of Choi and are inconsistent with the disclosure in Figures 1-3 of Choi and associated text upon which the Examiner relies in his *Graham* analysis. Any attempt to by the Examiner to interpret the disclosure in Figures 1-3 of Choi based upon the passages from the Background and Summary sections of Choi leads to irreconcilable inconsistencies. Again, the Appellant respectfully submits that the disclosure in Choi is more susceptible to the interpretation ascribed to the disclosure in Figures 1-3 of Choi, as explained herein and as explained in the Appellant's October 4, 2010 Appeal Brief, that the embodiment shown in Figures 1-3 of Choi should be interpreted as showing a functional transistor that includes only a single nanotube (100), and that

the Examiner's construction that the embodiment shown in Figures 1-3 of Choi includes multiple nanotubes is objectively unreasonable.

The Appellant respectfully submits that the Examiner has failed to establish a *prima facie* case of obviousness as to the pending claims, and as such, the Board should reverse the rejections under 35 U.S.C. § 103(a).

IV. Conclusion

For the reasons set forth in the Appellant's October 4, 2010 Appeal Brief and the reasons set forth herein, the Appellant respectfully requests that the Board reverse the Examiner's rejections of claims 1-6 and 8, and that the application be passed to issue. If there are any questions regarding the foregoing, please contact Appellant's undersigned representative. Moreover, if any other charges or credits are necessary to complete this communication, please apply them to Deposit Account 23-3000.

Respectfully submitted,
WOOD, HERRON & EVANS, L.L.P.

Date: February 2, 2011

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